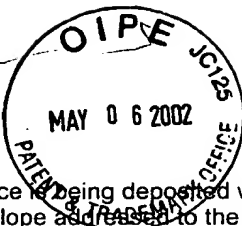


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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on the date indicated below.

By: [Signature]

Date: April 29, 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Karl Schrödinger
Applic. No. : 09/992,281
Filed : November 16, 2001
Title : Method and Apparatus for Producing a Clock Output Signal
Art Unit : 2859

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

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Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

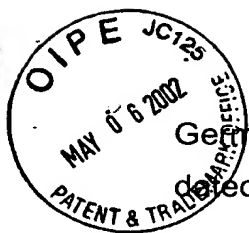
United States Patent No. 5,970,110 (Li), dated October 19, 1999;

German Patent DE 198 34 416 C2 (Miyano), dated February 4, 1999, clock signal generator;

German Patent DE 199 34 501 C1 (Heyne et al.), dated November 9, 2000, synchronous integral memory;

German Published, Non-Prosecuted Patent Application DE 39 14 249 A1 (Rudolph), dated December 13, 1990, method and circuit for automatic clock retrieval;

German Published, Non-Prosecuted Patent Application DE 39 40 860 A1 (Lenz et al.), dated June 13, 1991, circuit configuration for recognizing the TV signal;



German Published, Non-Prosecuted Patent Application DE 195 34 516 A1 (Rantakari),
dated March 14, 1996, phase lock loop circuit;

German Published, Non-Prosecuted Patent Application DE 197 01 937 A1 (Kim),
dated July 31, 1997, phase delay correction device;

German Published, Non-Prosecuted Patent Application DE 197 03 986 A1 (Kondoh et
al.), dated December 4, 1997, signal shaper for input clock signal device;

German translation of European Patent EP 0 304 791 B1 (Tateishi), dated March 1,
1989, phase-locked loop having elongated charge and discharge time;

German Published, Non-Prosecuted Patent Application DE 0 512 621 B1 (Dijkhof),
dated November 11, 1992, digital phase locked loop, and digital oscillator arranged to
be used in the digital phase locked loop;

European Patent Application EP 0 881 774 A2 (O'Sullivan), dated December 2, 1998;

German Examination Report dated February 6, 2002.

In accordance with 37 C.F.R. 1.97(e) the undersigned herewith states that each item of
information contained in the information disclosure statement was cited in a



communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,



For Applicant

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Date: April 29, 2002

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